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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2811

Applicant:	SHEN	Examiner:	Parekh, N.
Serial No.:	09/407,204	Group Art Unit:	2811
Filed:	September 28, 1999	Docket:	8688.128US01
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Title:	SEMICONDUCTOR CHIP MODULE		

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By: _____
Name: ~~John Junkins~~ STEVEN ENDRES JR

Commissioner for Patents
Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Communication Regarding Priority Document
- ☒ Certified English Translation of Priority Application Taiwan Application No. 88212813
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Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402-0903
612.332.5300

By: _____
Name: Bryan A. Wong
Reg. No.: 50,836
MDS/BAW/tlp

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By: _____
Name: ~~John Junkins~~ Steven Endres Jr.

#14 Translation FJones 5-30-02

COMMUNICATION REGARDING PRIORITY DOCUMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In connection with the above referenced patent application and in further response to the Response filed March 25, 2002, Applicant respectfully submits a certified English translation of the priority application Taiwan Patent Application No. 88212813.

If any further questions arise regarding this communication, the Examiner is invited to contact Applicant's representative at the number listed below.

Respectfully Submitted,

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

Dated: May 20, 2002

By _____
Bryan A. Wong
Reg. No. 50,836

MDS/BAW/tlp

VERIFICATION OF TRANSLATION

I, the below named translator, thereby declare that:

My name and post office address are as stated below:

That I am knowledgeable in the English language and in the Chinese language, and that I believe the attached English translation is a true and complete translation of the corresponding R.O.C. patent application as filed.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, and that such willful false statements may jeopardize the validity of the patent application or any patent issued thereon.

Date: April 19, 2002

Name of Translator: Kuan-Lai Wong

Signature of Translator:

Post Office Address: 7/F, No. 248, Nanking East Road, Section 3, Taipei City
Taiwan, R.O.C.

ABSTRACT

(Title: STACKED-TYPE MEMORY MODULE STRUCTURE AND MULTI-LAYER STACKED-TYPE MEMORY MODULE STRUCTURE EMPLOYING THE SAME)

A stacked-type memory module structure is adapted for mounting on a printed circuit board. The stacked-type memory module structure includes: a chip-mounting member, the chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, the first and second mounting surfaces having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on the hole-defining walls of the electroplated through holes; at least two chips, each of the chips having a bonding pad-mounting surface provided with a plurality of bonding pads; at least two insulating adhesive tape layers, the insulating adhesive tape layers being respectively disposed between one of the chips and the first mounting surface of the chip-mounting member and between the other one of the chips and the second mounting surface of the chip-mounting member, each of the insulating adhesive tape layers having a first adhesive surface adhered onto the bonding pad-mounting surface of the corresponding chip and a second adhesive surface adhered onto the corresponding mounting surface of the chip-mounting

member, the adhesive tape layers being formed with a plurality of through holes communicating the bonding pads on each of the chips and the corresponding circuit traces on the corresponding mounting surface of the chip-mounting member, a conductive metal ball being disposed in each of the through holes for establishing electrical connection between the bonding pads of the chips and the corresponding circuit traces of the chip-mounting member; and a plurality solder balls adapted to be mounted on the printed circuit board, the solder balls being disposed on one of the mounting surfaces of the chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on the hole-defining walls of the electroplated through holes.

FOREIGN FILING PARTICULARS

NONE

The invention relates to a stacked-type memory module structure and a multi-layer stacked-type memory module structure employing the same, more particularly to a stacked-type memory module structure that permits automated production and a multi-layer stacked-type memory module structure employing the same.

With the on-going progress of computer technology, computers operate at increasing speeds and have more powerful functions. As a result, there is a need for increased memory capacity. However, as the area of a main board is limited, an increased amount of memories will definitely take up the valuable area of the main board. Therefore, a stacked-type memory module construction has been developed to increase the memory capacity without occupying the area of the main board.

A conventional stacked-type memory module construction is such as that disclosed in USP 4,996,587 issued to IBM. However, as the means disclosed in the aforesaid U.S. patent additionally requires S-shaped connector clips that have to be manually assembled, automated manufacturing is not possible, thereby complicating the manufacturing process and increasing the overall costs to a considerable extent.

In view of the foregoing, the inventor, with years of experience in the industry and adhering to the spirit for advancement, indulged in research and improvement and finally came up with "A stacked-type memory module structure and a multi-layer stacked-type memory module structure

employing the same" of the present invention.

The object of the present invention is to provide a stacked-type memory module structure that can be manufactured in an automated manner and a multi-layer stacked-type memory module structure employing the same.

According to one aspect of the present invention, a stacked-type memory module structure is adapted for mounting on a printed circuit board. The stacked-type memory module structure includes: a chip-mounting member, the chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, the first and second mounting surfaces having predetermined circuit traces distributed thereon, which extend to corresponding electroplated through holes and which are connected electrically to the conductive material on the hole-defining walls of the electroplated through holes; at least two chips, each of the chips having a bonding pad-mounting surface provided with a plurality of bonding pads; at least two insulating adhesive tape layers, the insulating adhesive tape layers being respectively disposed between one of the chips and the first mounting surface of the chip-mounting member and between the other one of the chips and the second mounting surface of the chip-mounting member, and each having a first adhesive surface adhered onto the bonding pad-mounting surface of the corresponding one of the chips

and a second adhesive surface adhered onto the corresponding mounting surface of the chip-mounting member, the adhesive tape layers being formed with a plurality of through holes for communicating the bonding pads on each of the chips with the corresponding circuit traces of the corresponding mounting surface of the chip-mounting member, a conductive metal ball being disposed in each of the through holes to establish electrical connection between the bonding pads of the chips and the corresponding circuit traces of the chip-mounting member; and a plurality of solder balls adapted to be mounted on the printed circuit board, the solder balls being provided on one of the mounting surfaces of the chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on the hole-defining walls of the electroplated through holes.

According to another aspect of the present invention, a multi-layer stacked-type memory module structure is adapted for mounting on a printed circuit board. The multi-layer stacked-type memory module structure includes at least two stacked-type memory module structures. Each of the stacked-type memory module structures includes: a chip-mounting member, the chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, the first and second mounting surfaces having

predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on the hole-defining walls of the electroplated through holes; at least two chips, each of the chips having a bonding pad-mounting surface provided with a plurality of bonding pads; at least two insulating adhesive tape layers, the insulating adhesive tape layers being respectively disposed between one of the chips and the first mounting surface of the chip-mounting member and between the other one of the chips and the second mounting surface of the chip-mounting member, each of the insulating adhesive tape layers having a first adhesive surface adhered onto the bonding pad-mounting surface of the corresponding one of the chips and a second adhesive surface adhered onto the corresponding one of the mounting surfaces of the chip-mounting member, the adhesive tape layers being formed with a plurality of through holes communicating the bonding pads on each of the chips with the corresponding circuit traces on the corresponding one of the mounting surfaces of the chip-mounting member, a conductive metal ball being disposed in each of the through holes for establishing electrical connection between the bonding pads of the chips and the corresponding circuit traces of the chip-mounting member; and a plurality of solder balls adapted to be mounted on the printed circuit board, the solder balls being disposed on one of the mounting surfaces of the chip-mounting member, being in alignment

with the corresponding electroplated through holes, and being connected electrically to the conductive material on the hole-defining walls of the electroplated through holes.

The technical means adopted in the present invention to achieve the aforesaid objects and features, and the effects thereof are illustrated by way of preferred embodiments with reference to the accompanying drawings, of which:

Figure 1 is a schematic sectional view depicting the first preferred embodiment of a stacked-type memory module structure according to the present invention;

Figure 2 is a schematic perspective view of a chip-mounting member of the first preferred embodiment of the present invention in part;

Figure 3 is a schematic perspective view of a chip of the first preferred embodiment of the present invention in part;

Figure 4 is a schematic perspective view of an adhesive tape layer of the first preferred embodiment of the present invention in part;

Figure 5 is a schematic sectional view of a multi-layer stacked-type memory module structure that employs the first preferred embodiment of the present invention;

Figure 6 is a schematic sectional view of the second preferred embodiment of the present invention;

Figure 7 is a schematic sectional view of a multi-layer stacked-type memory module structure that employs the second preferred embodiment of the present invention;

Figure 8 is a schematic sectional view of the third preferred embodiment of the present invention;

Figure 9 is a schematic sectional view of a multi-layer stacked-type memory module structure that employs the third preferred embodiment of the present invention;

Figure 10 is a schematic sectional view of the fourth preferred embodiment of the present invention;

Figure 11 is a schematic sectional view of a multi-layer stacked-type memory module structure that employs the fourth preferred embodiment of the present invention; and

Figure 12 is a side view illustrating the fifth preferred embodiment of the present invention.

LIST OF REFERENCE NUMERALS

1	chip-mounting member	2	chip
3	solder ball	4	adhesive tape layer
5	conductive metal ball	10	first mounting surface
11	second mounting surface	12	circuit traces
14	electroplated through hole	23	epoxy resin layer
20	bonding pad-mounting surface	21	bonding pad
22	lead wire	40	through hole
13	cavity	6	encapsulation layer
4a	insulating adhesive tape layer	13a	cavity
2a	first chip	2b	second chip
24	heat-dissipating plate	1a	first chip-mounting

			member
1b	second chip-mounting member	3a	first solder ball
17a	through hole	15a	chip-mounting surface
15b	chip-mounting surface	16a	circuit trace layout surface
16b	circuit trace layout surface	14a	electroplated through hole
14b	electroplated through hole	23a	epoxy resin layer
23b	epoxy resin layer	24a	metal heat-dissipating plate
24b	metal heat-dissipating plate	20a	bonding pad-mounting surface
20b	bonding pad-mounting surface	21a	bonding pad
21b	bonding pad	22a	lead wire
22b	lead wire	6a	encapsulation layer
6b	encapsulation layer	7	first insulating adhesive tape layer
70	through hole	8	second insulating adhesive tape layer
80	through hole		

Before the present invention is described in greater detail, it should be noted that like elements are denoted by the same reference numerals throughout the disclosure.

Referring to Figure 1, the first preferred embodiment

of a stacked-type memory module structure according to the present invention is shown to comprise a chip-mounting member 1, at least two chips 2, and a plurality of solder balls 3.

In this embodiment, the chip-mounting member 1 is a substrate board having a first mounting surface 10 and a second mounting surface 11. Predetermined circuit traces 12 (see Figure 2) are laid out on the first and second mounting surfaces 10, 11. The chip-mounting member 1 is formed with a plurality of electroplated through holes 14 with hole-defining walls that are electroplated with a conductive material. The circuit traces 12 on the first and second surfaces 10, 11 of the chip-mounting member 1 extend to the corresponding through holes 14 and are connected electrically to the conductive material on the hole-defining walls.

Each of the chips 2 has a bonding pad-mounting surface 20 (see Figure 3). The bonding pad-mounting surface 20 has a plurality of bonding pads 21 disposed thereon. The chips 2 are mounted respectively on the first and second mounting surfaces 10, 11 of the chip-mounting member 1 via insulating adhesive tape layers 4, each of which has first and second adhesive surfaces. The first adhesive surface of each of the insulating adhesive tape layers 4 is adhered onto the bonding pad-mounting surface 20 of the corresponding one of the chips 2, whereas the second adhesive surface thereof is adhered onto a corresponding one of the mounting surfaces

10, 11 of the chip-mounting member 1. The adhesive tape layer 4 is formed with a plurality of through holes 40 (see Figure 4) for communicating the bonding pads 21 on the chips 2 with the corresponding traces 12 on the corresponding mounting surfaces 10, 11 of the chip-mounting member 1. Electrical connection between the bonding pads 20 [sic] of the chips 2 and the corresponding traces 12 on the chip-mounting member 1 is established via conductive metal balls 5 disposed in the through holes 40. An epoxy resin layer 23 is further formed between the periphery of each of the chips 2 and the corresponding one of the mounting surfaces 10, 11 of the chip-mounting member 1 to further secure the chips 2. It should be noted that, for purposes of dissipating heat and protecting the chips 2, a metal heat-dissipating plate 24 can be further provided between a surface of each of the chips 2 that is opposite to the bonding pad-mounting surface 20.

The solder balls 3 (only two are illustrated in Figure 1) are disposed on the second mounting surface 11 of the chip-mounting member 1, are in alignment with the corresponding electroplated through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14 such that the solder balls 3 are connected electrically to the corresponding bonding pads 21 of the chips 2 via the circuit traces 12 on the mounting surfaces 10, 11 of the chip-mounting member 1.

It should be noted that, although the drawing of the preferred embodiment shows that there is only one chip 2 on each of the first and second mounting surfaces 10, 11 of the chip-mounting member 1, it should be apparent to those skilled in the art that two or more chips 2 may be provided on each of the first and second mounting surface 10, 11 of the chip-mounting member 1.

With further reference to Figure 5, a multi-layer stacked-type memory module structure employing the first preferred embodiment of the present invention is shown to comprise a plurality of the stacked-type memory module structures of the first preferred embodiment of the present invention. The solder balls 3 on an upper one of the memory module structures are secured on the first mounting surface 10 of the chip-mounting member 1 of a lower one of the memory module structures, are in alignment with the corresponding through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14. The solder balls 3 on the lowermost one of the memory module structures are adapted to be secured on a printed circuit board (not shown) and are connected electrically to corresponding circuit traces on the printed circuit board.

Reference is made to Figure 6, which shows the second preferred embodiment of the present invention. In this embodiment, the chip-mounting member 1 is a three-layer substrate board, and each of the first and second mounting

surfaces 10, 11 is provided with at least one chip-receiving cavity 13 for receiving the chip 2. A surface of each of the chips 2 that is opposite to the bonding pad-mounting surface 20 is adhered onto a first adhesive surface of an insulating adhesive tape layer 4a. The insulating adhesive tape layer 4a has a second adhesive surface adhered onto a bottom wall of the corresponding cavity 13 of the chip-mounting member 1, whereby each of the chips 2 can be secured in the corresponding cavity 13. Unlike the first preferred embodiment, the adhesive tape layer 4a is not formed with through holes for exposing the bonding pads 21 of the chip 2. The bonding pads 21 of the chips 2 are connected electrically to the corresponding circuit traces, such as those shown in Figure 2, on the corresponding mounting surfaces 10, 11 of the chip-mounting member 1 via lead wires 22. In addition, an encapsulation layer 6 is provided on each of the first and second mounting surfaces 10, 11 of the chip-mounting member 1 to cover the lead wires 22 and the bonding pad-mounting surface 20 of the chip 2 for protective purposes. The encapsulation layer 6 may be formed from epoxy resin.

Similar to the first preferred embodiment, the solder balls 3 are disposed on the second mounting surface 11 of the chip-mounting member 1, are in alignment with the corresponding electroplated through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes. As such, the

solder balls 3 are connected electrically to the corresponding bonding pads 21 of the chips 2 via the circuit traces on the mounting surfaces 10, 11 of the chip-mounting member 1 and the lead wires 22.

With further reference to Figure 7, a multi-layer stacked-type memory module structure employing the second preferred embodiment of the present invention is shown to comprise a plurality of the stacked-type memory module structures according to the second preferred embodiment of the present invention, similar to the structure shown in Figure 5. The solder balls 3 on an upper one of the memory module structures are secured on the first mounting surface 10 of the chip-mounting member 1 of a lower one of the memory module structures, are in alignment with the corresponding electroplated through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14. The solder balls 3 on the lowermost one of the memory module structures are adapted to be secured to a printed circuit board (not shown), and are connected electrically to corresponding circuit traces on the printed circuit board.

Reference is made to Figure 8, which shows the third preferred embodiment of the present invention. The third preferred embodiment is shown to include a chip-mounting member 1, at least two first chips 2a, at least two second chips 2b, at least two first insulating adhesive tape layers 4, at least two second insulating adhesive tape layers 4a,

and a plurality of solder balls 3.

In this embodiment, the chip-mounting member 1 is a three-layer substrate board having first and second mounting surfaces 10, 11. Each of the mounting surfaces 10, 11 is formed with at least one chip-receiving cavity 13a for receiving chips. On the other hand, predetermined circuit traces, such as those shown in Figure 2, are laid out on each of the mounting surfaces 10, 11 and on the bottom wall of each of the cavities 13a. Each of the circuit traces extends to the corresponding electroplated through hole 14 formed in the chip-mounting member 1.

Each of the first chips 2a is received in the corresponding cavity 13a, and has a bonding pad-mounting surface 20 provided with a bonding pad 21 and adhered onto the first adhesive surface of the first insulating adhesive tape layer 4. The second adhesive surface of the first insulating adhesive tape layer 4 is adhered onto the bottom wall of the corresponding cavity 13a. Similar to the first embodiment, the first adhesive tape layer 4 is formed with a plurality of through holes 40 for communicating the bonding pads 21 of the chips 2a with the corresponding circuit traces on the bottom walls of the corresponding cavities 13a. Electrical connection between the bonding pads 21 on the chips 2a and the circuit traces on the bottom walls of the corresponding cavities 13a is established via conductive metal balls 5.

Each of the second chips 2b is received in the

corresponding cavity 13a. A surface thereof that is opposite to the bonding pad-mounting surface 20 with the bonding pads 21 is adhered onto the first adhesive surface of the second insulating adhesive tape layer 4a. The second adhesive surface of the second adhesive tape layer 4a is adhered onto the surface of a corresponding one of the first chips 2a that is opposite to the bonding pad-mounting surface 20. Like the second preferred embodiment, electrical connection between the bonding pads 21 of each of the second chips 2b and the circuit traces on the corresponding mounting surface 10, 11 of the chip-mounting member 1 is established via lead wires 22.

The solder balls 3 are disposed on the second mounting surface 11 of the chip-mounting member 1, are in alignment with the corresponding electroplated through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14. As such, the solder balls 3 are connected electrically to the corresponding bonding pads 21 of the second chips 2b via the circuit traces on the mounting surfaces 10, 11 of the chip-mounting member 1 and the lead wires 22, and to the corresponding bonding pads 21 of the first chips 2a via the circuit traces on the bottom walls of the cavities 13a.

With further reference to Figure 9, a multi-layer stacked-type memory module structure employing the third preferred embodiment is shown to include a plurality of the stacked-type memory module structures according to the third

preferred embodiment of the present invention. Like the structure illustrated in Figure 5, solder balls 3 on an upper one of the memory module structures are secured on the first mounting surface 10 of the chip-mounting member 1 of a lower one of the memory module structures, are in alignment with the corresponding electroplated through holes 14, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14. Solder balls 3 on the lowermost one of the memory module structures are adapted to be mounted on a printed circuit board (not shown), and are connected electrically to corresponding circuit traces on the printed circuit board.

Referring to Figure 10, the fourth preferred embodiment of a stacked-type memory module structure according to the present invention is shown to include first and second chip-mounting members 1a, 1b, at least one first chip 2a, at least one second chip 2b, a plurality of first solder balls 3a, and a plurality of second solder balls 3.

The first chip-mounting member 1a has a chip-mounting surface 15a and a circuit trace layout surface 16a opposite to the chip-mounting surface 15a. The first chip-mounting member 1a is formed with a through hole 17a for exposing the bonding pads of the chip, and a plurality of electroplated through holes 14a having hole-defining walls electroplated with a conductive material. The circuit trace layout surface 16a has predetermined circuit traces, such as those shown in Figure 2, laid out thereon, which extend to the

corresponding electroplated through holes 14a and which are connected electrically to the conductive material on the hole-defining walls of the through holes 14a.

The second chip-mounting member 1b has a chip-mounting surface 15b and a circuit trace layout surface 16b opposite to the chip-mounting surface 15b. The second chip-mounting member 1b is formed with a through hole 17b for exposing the bonding pads of the chip, and a plurality of electroplated through holes 14b having hole-defining walls electroplated with a conductive material. Predetermined circuit traces, such as those shown in Figure 2, are laid out on the circuit trace layout surface 16b to extend to the corresponding electroplated through holes 14b, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14b.

The first chip 2a has a bonding pad-mounting surface 20a with bonding pads 21a mounted thereon. The bonding pad-mounting surface 20a of the first chip 2a is adhered onto a first adhesive surface of a first insulating adhesive tape layer 7. The first insulating adhesive tape layer 7 has a second adhesive surface adhered onto the chip-mounting surface 15a of the first chip-mounting member 1a. The first insulating adhesive tape layer 7 is formed with a through hole 70 aligned with the through hole 17a in the chip-mounting member 1a. The bonding pads 21a of the first chip 2a are connected electrically to the corresponding circuit traces on the circuit trace layout surface 16a of the first

chip-mounting member 1a via lead wires 22a. In addition, an encapsulation layer 6a is provided on the circuit trace layout surface 16a of the first chip-mounting member 1a for covering the lead wires 22a and exposed portions of the bonding pad-mounting surface 20a of the first chip 2a for protection purposes. The encapsulation layer 6a may be formed from epoxy resin.

Similar to the first embodiment, an epoxy resin layer 23a is formed between the periphery of the first chip 2a and the chip-mounting surface 15a of the first chip-mounting member 1a to further secure the chip 2a. At the same time, a surface of the first chip 2a that is opposite to the bonding pad-mounting surface 20a is provided with a metal heat-dissipating plate 24a.

The second chip 2a has a bonding pad-mounting surface 20b provided with bonding pads 21b. The bonding pad-mounting surface 20b of the second chip 2b is adhered onto a first adhesive surface of a second insulating adhesive tape layer 8. The second insulating adhesive tape layer 8 has a second adhesive surface adhered onto the chip-mounting surface 15b of the second chip-mounting member 1b. The second insulating adhesive tape layer 8 is formed with a through hole 80 aligned with the through hole 17b in the chip-mounting member 1b. The bonding pads 21b of the second chip 2b are connected electrically to the corresponding circuit traces on the circuit trace layout surface 16b of the second chip-mounting member 1b via lead wires 22b. In

addition, an encapsulation layer 6b is provided on the circuit trace layout surface 16b of the second chip-mounting member 1b for covering the lead wires 22b and exposed portions of the bonding pad-mounting surface 20b of the second chip 2b for protection purposes. The encapsulation layer 6b may be formed from epoxy resin.

Similar to the first embodiment, an epoxy resin layer 23b is formed between the periphery of the second chip 2b and the chip-mounting surface 15b of the second chip-mounting member 1b to further secure the chip 2b. At the same time, a surface of the first [sic] chip 2b that is opposite to the bonding pad-mounting surface 20b is provided with a metal heat-dissipating plate 24b.

The first solder balls 3a are disposed between the first and second chip-mounting members 1a, 1b. Each of the solder balls 3a is aligned with the corresponding electroplated through hole 14a in the first chip-mounting member 1a and the corresponding electroplated through hole 14b in the second chip-mounting member 1b, and is connected electrically to the conductive material on the hole-defining walls of the through holes 14a, 14b. As such, the first solder balls 3a are connected electrically to the corresponding bonding pads 21a, 21b of the chips 2a, 2b via the circuit traces on the circuit trace layout surfaces 16a, 16b of the chip-mounting members 1a, 1b and the lead wires 22a, 22b.

The second solder balls 3 are disposed on the chip-

mounting surface 15b of the second chip-mounting member 1b, are in alignment with the corresponding electroplated through holes 14b, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14b.

Referring to Figure 11, a multi-layer stacked-type memory module structure employing the fourth preferred embodiment of the present invention is shown to include a plurality of the stacked-type memory module structures according to the fourth preferred embodiment of the present invention. Similar to the structure shown in Figure 5, the second solder balls 3 of an upper one of the memory module structures are secured on the chip-mounting surface 15a of the first chip-mounting member 1a of a lower one of the memory module structures, are in alignment with corresponding electroplated through holes 14a, and are connected electrically to the conductive material on the hole-defining walls of the through holes 14a. The second solder balls 3 of the lowermost one of the memory module structures are adapted to be mounted on a printed circuit board (not shown), and are connected electrically to corresponding circuit traces on the printed circuit board.

Reference is made to Figure 12, which shows the fifth preferred embodiment of the present invention. Unlike the fourth embodiment, the embodiment of Figure 12 shows that each of the chip-mounting members 1a, 1b has at least two chips 2a, 2b mounted thereon.

To sum up, the stacked-type memory module structure and the multi-layer stacked-type memory module structure utilizing the same of the present invention can indeed achieve the intended objects and effects by virtue of the construction and devices disclosed hereinabove, and were not disclosed in any printed publication or put to public use prior to filing, thereby complying with the patentability requirements of novelty and inventive step.

It is noted that the aforesaid is intended to illustrate the preferred embodiments of the present invention and not to limit the scope of the present invention. Any equivalent arrangements or modifications made by those skilled in the art within the scope of the present invention should be deemed to fall within the scope of the claims of the subject application.

CLAIMS:

1. A stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, said first and second mounting surfaces having predetermined circuit traces laid out thereon, which extend to corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

at least two chips, each of said chips having a bonding pad-mounting surface provided with a plurality of bonding pads;

at least two insulating adhesive tape layers, said insulating adhesive tape layers being respectively disposed between one of said chips and said first mounting surface of said chip-mounting member and between the other one of said chips and said second mounting surface of said chip-mounting member, and each having a first adhesive surface adhered onto said bonding pad-mounting surface of the corresponding one of said chips and a second adhesive surface adhered onto the corresponding mounting surface of said chip-mounting member, said adhesive tape layers being formed with a plurality of through holes for communicating said bonding pads on each of said chips with the corresponding

circuit traces of the corresponding mounting surface of said chip-mounting member, a conductive metal ball being disposed in each of said through holes to establish electrical connection between said bonding pads of said chips and the corresponding circuit traces of said chip-mounting member; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being provided on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said electroplated through holes.

2. The stacked-type memory module structure as claimed in Claim 1, wherein an epoxy resin layer is formed between a periphery of each of said chips and the corresponding mounting surface of said chip-mounting member.

3. The stacked-type memory module structure as claimed in Claim 1, wherein a metal heat-dissipating plate is disposed on the surface of each of said chips that is opposite to said bonding pad-mounting surface thereof.

4. A stacked-type memory module structure adapted to be mounted on a printed circuit board, comprising:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive

material, each of said first and second mounting surfaces being provided with at least one chip-receiving cavity and both having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

at least two chips, each of said chips having a bonding pad-mounting surface provided with a plurality of bonding pads, said chips being respectively disposed in the corresponding chip-receiving cavities in said chip-mounting member;

at least two insulating adhesive tape layers, said insulating adhesive tape layers being respectively provided between one of said chips and a bottom wall of one of said cavities in said chip-mounting member and between the other one of said chips and a bottom wall of the other one of said cavities in said chip-mounting member, each of said adhesive tape layers having a first adhesive surface adhered onto the surface of the corresponding one of said chips that is opposite to said bonding pad-mounting surface, and a second adhesive surface adhered onto said bottom wall of the corresponding cavity in said chip-mounting member, said bonding pads of said chips being connected electrically to said circuit traces on the corresponding mounting surface of said chip-mounting member via lead wires;

at least two encapsulation layers, said encapsulation

layers being disposed to cover said bonding pad-mounting surfaces of the corresponding chips and said lead wires; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being disposed on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said electroplated through holes.

5. The stacked-type memory module structure as claimed in Claim 4, wherein said encapsulating layer is formed from epoxy resin.

6. A stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, said first and second mounting surfaces being respectively provided with at least one chip-receiving cavity, said first and second mounting surfaces and a bottom wall of each of said cavities having predetermined circuit traces laid out thereon, which extend to corresponding electroplated through holes and which are connected electrically to the conductive material on the hole-defining walls of the electroplated through holes;

at least two first chips, each of said first chips having

a bonding pad-mounting surface provided with a plurality of bonding pads, said first chips being respectively received in the corresponding chip-receiving cavity in said chip-mounting member;

at least two first insulating adhesive tape layer, said first insulating adhesive tape layers being respectively disposed between one of said chips and a bottom wall of the corresponding cavity in said chip-mounting member and between the other one of said chips and a bottom wall of the corresponding cavity in the chip-mounting member, each of said first adhesive tape layers having a first adhesive surface adhered onto the bonding pad-mounting surface of the corresponding chip and a second adhesive surface adhered onto the bottom wall of the corresponding cavity in said chip-mounting member, said first adhesive tape layers being formed with a plurality of through holes for communicating said bonding pads on each of said first chips and the corresponding circuit traces on the bottom wall of the corresponding cavity in said chip-mounting member, each of said through holes having a conductive metal ball disposed therein to establish electrical connection between said bonding pads of said first chips and said circuit traces on the bottom wall of the corresponding cavity in said chip-mounting member;

at least two second chips, each of said second chips having a bonding pad-mounting surface provided with a plurality of bonding pads, said second chips being

respectively received in the corresponding chip-receiving cavities in said chip-mounting member;

at least two second insulating adhesive tape layers, said second insulating adhesive tape layers being disposed respectively between one of said first chips and the corresponding one of said second chips and between the other one of said first chips and the corresponding one of said second chips, said second adhesive taper layers respectively having a first adhesive surface adhered onto a surface of the corresponding one of said second chips that is opposite to said bonding pad-mounting surface thereof and a second adhesive surface adhered onto a surface of the corresponding one of said first chips that is opposite to said bonding pad-mounting surface thereof, said bonding pads of said second chips being connected electrically to said circuit traces on the corresponding mounting surfaces of said chip-mounting member via lead wires;

at least two encapsulation layers, said encapsulation layers being disposed to cover said bonding pad-mounting surfaces of the corresponding second chips and said lead wires; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being disposed on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said

electroplated through holes.

7. The stacked-type memory module structure as claimed in Claim 6, wherein said encapsulation layers are formed from epoxy resin.

8. A stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

first and second chip-mounting members, each of said chip-mounting members having a chip-mounting surface and a circuit trace layout surface opposite to said chip-mounting surface, each of said chip-mounting members being formed with a through hole for exposing bonding pads of a chip, and a plurality of electroplated through holes with hole-defining walls electroplated with a conductive material, said circuit trace layout surface of each of said chip-mounting members having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

a first chip, said first chip having a bonding pad-mounting surface having bonding pads mounted thereon, said bonding pad-mounting surface of said first ship being adhered onto a first adhesive surface of a first insulating adhesive tape layer, said first insulating adhesive tape layer having a second adhesive surface adhered onto said chip-mounting surface of said first chip-mounting member, said first insulating adhesive tape layer being formed with

a through hole that is aligned with said through hole in said chip-mounting member, said bonding pads of said first chip being connected electrically to the corresponding circuit traces on said circuit trace layout surface of said first chip-mounting member via lead wires, said circuit trace layout surface of said first chip-mounting member being provided with an encapsulation layer for covering said lead wires and exposed portions of said bonding pad-mounting surface of said first chip;

a second chip, said second chip having a bonding pad-mounting surface having bonding pads mounted thereon, said bonding pad-mounting surface of said second chip being adhered onto a first adhesive surface of a second insulating adhesive tape layer, said second insulating adhesive tape layer having a second adhesive surface adhered onto said chip-mounting surface of said second chip-mounting member, said second insulating adhesive tape layer being formed with a through hole in alignment with said through hole in said second chip-mounting member, said bonding pads of said second chip being connected electrically to corresponding circuit traces on the circuit trace layout surface of said second chip-mounting member via lead wires, said circuit trace layout surface of said second chip-mounting member being provided with an encapsulation layer for covering said lead wires and exposed portions of said bonding pad-mounting surface of said second chip;

a plurality of first solder balls, said first solder balls

being placed between said first and second chip-mounting members, each of said first solder balls being aligned with a corresponding one of said electroplated through holes in said first chip-mounting member and a corresponding one of said electroplated through holes in said second chip-mounting member, and being connected electrically to the conductive material on said hole-defining walls of said through holes, such that each of said first solder balls is connected electrically to the corresponding bonding pad of said first and second chips via said circuit traces on said circuit trace layout surface of said chip-mounting members and said lead wires; and

a plurality of second solder balls, said second solder balls being disposed between said chip-mounting surface of said second chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said through holes.

9. The stacked-type memory module structure as claimed in Claim 8, wherein said encapsulation layer is formed from epoxy resin.

10. The stacked-type memory module structure as claimed in Claim 8, wherein an epoxy resin layer is formed between a periphery of said first chip and said chip-mounting surface of said first chip-mounting member.

11. The stacked-type memory module structure as claimed in Claim 8, wherein a metal heat-dissipating plate is disposed

on the surface of said first chip that is opposite to said bonding pad-mounting surface thereof.

12. The stacked-type memory module structure as claimed in Claim 8, wherein an epoxy resin layer is formed between a periphery of said second chip and said chip-mounting surface of said second chip-mounting member.

13. The stacked-type memory module structure as claimed in Claim 8, wherein a metal heat-dissipating plate is disposed on the surface of said second chip that is opposite to said bonding pad-mounting surface thereof.

14. A multi-layer stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

at least two stacked-type memory module structures, each of said stacked-type memory module structures including:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, said first and second mounting surfaces having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

at least two chips, each of said chips having a bonding pad-mounting surface provided with a plurality of bonding pads;

at least two insulating adhesive tape layers, said insulating adhesive tape layers being respectively disposed between one of said chips and said first mounting surface of said chip and between the other one of said chips and said second mounting surface of said chip-mounting member, each of said insulating adhesive tape layers having a first adhesive surface adhered onto said bonding pad-mounting surface of a corresponding one of said chips and a second adhesive surface adhered onto a corresponding one of said mounting surfaces, said adhesive tape layers being formed with a plurality of through holes communicating said bonding pads of each of said chips and the corresponding circuit traces on a corresponding one of said mounting surfaces of said chip-mounting member, a conductive metal ball being disposed in each of said through holes for establishing electrical connection between said bonding pads of said chips and the corresponding circuit traces of said chip-mounting member; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being disposed on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said electroplated through holes.

15. The multi-layer stacked-type memory module structure as claimed in Claim 14, wherein an epoxy resin layer is formed

between a periphery of each of said chips and a corresponding one of said mounting surfaces of said chip-mounting member.

16. The multi-layer stacked-type memory module structure as claimed in Claim 14, wherein a metal heat-dissipating plate is disposed on a surface of each of said chips that is opposite to said bonding pad-mounting surface.

17. A multi-layer stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

at least two stacked-type memory module structures, each of said stacked-type memory module structures comprising:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, each of said first and second mounting surfaces being provided with at least one chip-receiving cavity and having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

at least two chips, each of said chips having a bonding pad-mounting surface provided with a plurality of bonding pads, said chips being respectively received in the corresponding chip-receiving cavities in said chip-mounting member;

at least two insulating adhesive tape layers, said

insulating adhesive tape layers being respectively disposed between one of said chips and a bottom wall of one of said cavities in said chip-mounting member and between the other one of said chips and a bottom wall of the other one of said cavities in said chip-mounting member, each of said adhesive tape layers having a first adhesive surface adhered onto a surface of a corresponding one of said chips that is opposite to said bonding pad-mounting surface thereof and a second adhesive surface adhered onto the bottom wall of the corresponding one of said cavities in said chip-mounting member, said bonding pads of said chips being connected electrically to said circuit traces on the corresponding one of said mounting surfaces of said chip-mounting member via lead wires;

at least two encapsulation layers, said encapsulation layers being disposed to cover said bonding pad-mounting surface of a corresponding one of said chips and said lead wires; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being disposed on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said electroplated holes.

18. The multi-layer stacked-type memory module structure as claimed in Claim 17, wherein said encapsulation layers are

formed from epoxy resin.

19. A multi-layer stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

at least two stacked-type memory module structures, each of said stacked-type memory module structures comprising:

a chip-mounting member, said chip-mounting member having a first mounting surface and a second mounting surface, and being formed with a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, each of said first and second mounting surfaces being provided with at least one chip-receiving cavity, said first and second mounting surfaces and a bottom wall of each of said cavities having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

at least two first chips, each of said first chips having a bonding pad-mounting surface provided with a plurality of bonding pads, said first chips being respectively received in the corresponding chip-receiving cavities in said chip-mounting member;

at least two first insulating adhesive tape layers, said first insulating adhesive layers being respectively disposed between one of said chips and a bottom wall of the corresponding cavity in said chip-mounting member and between the other one of said chips and a bottom wall of the

corresponding cavity in said chip-mounting member, each of said first adhesive tape layers having a first adhesive surface adhered onto said bonding pad-mounting surface of a corresponding one of said chips and a second adhesive surface adhered onto said bottom wall of the corresponding cavity in said chip-mounting member, said first adhesive tape layers being formed with a plurality of through holes communicating said bonding pads of each of said first chips and the corresponding circuit traces on said bottom walls of the corresponding cavities in said chip-mounting member, a conductive metal ball being disposed in each of said through holes for establishing electrical connection between said bonding pads of said first chips and said circuit traces on said bottom walls of the corresponding cavities in said chip-mounting member;

at least two second chips, each of said second chips having a bonding pad-mounting surface provided with a plurality of bonding pads, said second chips being respectively received in the corresponding chip-receiving cavities in said chip-mounting member;

at least two second insulating adhesive tape layers, said second insulating adhesive tape layers being respectively disposed between one of said first chips and a corresponding one of said second chips and between the other one of said chips and a corresponding one of said second chips, each of said second adhesive tape layers having a first adhesive surface adhered onto a surface of the corresponding

one of said second chips that is opposite to said bonding pad-mounting surface thereof and a second adhesive surface adhered onto a surface of the corresponding one of said first chips that is opposite to said bonding pad-mounting surface thereof, said bonding pads of said second chips being connected electrically to said circuit traces on the corresponding mounting surfaces of said chip-mounting member via lead wires;

at least two encapsulation layers, said encapsulation layers being disposed to cover said bonding pad-mounting surface of the corresponding one of said second chips and said lead wires; and

a plurality of solder balls adapted to be mounted on the printed circuit board, said solder balls being disposed on one of said mounting surfaces of said chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said electroplated through holes.

20. The multi-layer stacked-type memory module structure as claimed in Claim 19, wherein said encapsulation layers are formed from epoxy resin.

21. A multi-layer stacked-type memory module structure adapted for mounting on a printed circuit board, comprising:

at least two stacked-type memory module structures, each of said stacked-type memory module structures comprising:

first and second chip-mounting members, each of said

chip-mounting members having a chip-mounting surface and a circuit trace layout surface opposite to said chip-mounting surface, each of said chip-mounting members being formed with a through hole for exposing bonding pads of chips and a plurality of electroplated through holes having hole-defining walls electroplated with a conductive material, said circuit trace layout surface of each of said chip-mounting members having predetermined circuit traces laid out thereon, which extend to the corresponding electroplated through holes and which are connected electrically to the conductive material on said hole-defining walls of said electroplated through holes;

a first chip, said first chip having a bonding pad-mounting surface that has bonding pads mounted thereon, said bonding pad-mounting surface of said first chip being adhered onto a first adhesive surface of a first insulating adhesive tape layer, said first insulating adhesive tape layer having a second adhesive surface adhered onto said chip-mounting surface of said first chip-mounting member, said first insulating adhesive tape layer being formed with a through hole that is aligned with said through hole in said chip-mounting member, said bonding pads of said first chip being connected electrically to the corresponding circuit traces on said circuit trace layout surface of said first chip-mounting member via lead wires, said circuit trace layout surface of said first chip-mounting member being provided with an encapsulation layer for covering said lead

wires and exposed portions of said bonding pad-mounting surface of said first chip;

a second chip, said second chip having a bonding pad-mounting surface that has bonding pads mounted thereon, said bonding pad-mounting surface of said second chip being adhered onto a first adhesive surface of a second insulating adhesive tape layer, said second insulating adhesive tape layer having a second adhesive surface adhered onto said chip-mounting surface of said second chip-mounting member, said second insulating adhesive tape layer being formed with a through hole aligned with said through hole in said second chip-mounting member, said bonding pads of said second chip being connected electrically to the corresponding circuit traces on said circuit trace layout surface of said second chip-mounting member via lead wires, said circuit trace layout surface of said second chip-mounting member being provided with an encapsulation layer for covering said lead wires and exposed portions of said bonding pad-mounting surface of said second chip;

a plurality of first solder balls, said first solder balls being disposed between said first and second chip-mounting members, each of said first solder balls being aligned with a corresponding one of said electroplated through holes in said first chip-mounting member and a corresponding one of said electroplated through holes in said second chip-mounting member, and being connected electrically to the conductive material on said hole-

defining walls of said through holes such that each of said first solder balls is connected electrically to the corresponding bonding pads of said first and second chips via said circuit traces on said circuit trace layout surfaces of said chip-mounting members and said lead wires; and

a plurality of second solder balls, said second solder balls being disposed on said chip-mounting surface of said second chip-mounting member, being in alignment with the corresponding electroplated through holes, and being connected electrically to the conductive material on said hole-defining walls of said through holes.

22. The multi-layer stacked-type memory module structure as claimed in Claim 21, wherein said encapsulation layers are formed from epoxy resin.

23. The multi-layer stacked-type memory module structure as claimed in Claim 21, wherein an epoxy resin layer is formed between a periphery of said first chip and said chip-mounting surface of said first chip-mounting member.

24. The multi-layer stacked-type memory module structure as claimed in Claim 21, wherein a metal heat-dissipating plate is disposed on a surface of said first chip that is opposite to said bonding pad-mounting surface thereof.

25. The multi-layer stacked-type memory module structure as claimed in Claim 21, wherein an epoxy resin layer is formed between a periphery of said second chip and said chip-mounting surface of said second chip-mounting member.

26. The multi-layer stacked-type memory module structure as

claimed in Claim 21, wherein a metal heat-dissipating plate is disposed on a surface of said second chip that is opposite to said bonding pad-mounting surface thereof.